WHAT IS CLAIMED IS:

1. A plasma display driving method wherein each frame comprises subfields; each of said subfields includes a reset period for performing an erase discharge to initialize a wall charge distribution in each cell, an address period for generating a wall charge distribution in accordance with display data, and a sustain discharge period for discharging in accordance with the wall charge distribution generated in the cell during said address period, to emit light; and

said reset period includes first and second erase discharge periods for performing erase discharges for cells having been turned on and not having been turned on, respectively.

2. A method according to claim 1, wherein a full-surface write discharge and a full-surface erase discharge are done during said reset period only in a specific subfield among the subfields in each frame, erase discharges for erasing wall charges accumulated in cells are done during said reset periods in the remaining subfields without performing said full-surface write discharges, and the erase discharges done separately in said first and second erase discharge periods are executed in the subfields except for said specific subfield.

3. A method according to claim 1, wherein the erase discharge in each said second erase discharge

period is achieved by applying to a first electrode a first erase pulse whose application voltage continuously changes with time in a positive direction, and applying to a second electrode a second erase pulse whose application voltage continuously changes with time in a negative direction.

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4. A ~~method according to claim 3,~~ wherein the pulse widths of said first and second erase pulses have time widths required to reach the ultimate voltages of said first and second erase pulses.

5. A method according to claim 3, wherein said first and second erase pulses have waveforms whose change rates per unit time of the application voltage change with time.

6. A method according to claim 3, wherein said first and second erase pulses have waveforms whose change rates per unit time of the application voltage are constant.

7. A method according to claim 3, wherein the potential difference between the ultimate voltages of said first and second erase pulses is around the discharge start voltage between said first and second electrodes and is smaller than said discharge start voltage.

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8. A method according to claim 7, wherein at least one of said ultimate voltages of said first and second erase pulses is variable.

9. ~~A method according to claim 3, wherein the~~ rise start timing of said first erase pulse is synchronized with or delayed from the fall start timing of said second erase pulse.

10. A plasma display driving apparatus for driving a plasma display panel in each of the subfields constituting one frame, each of said subfields including a reset period for performing an erase discharge to initialize a wall charge distribution in each cell, an address period for generating a wall charge distribution in accordance with display data, and a sustain discharge period for discharging in accordance with the wall charge distribution generated in the cell during said address period, to emit light, said apparatus comprising:

a controller for performing erase discharges for cells having been turned on and not having been turned on, in first and second erase discharge periods in said reset period, respectively.

11. An apparatus according to claim 10, wherein said controller performs a full-surface write discharge and a full-surface erase discharges during said reset period only in a specific subfield among the subfields in each frame, erase discharges for erasing wall charges accumulated in cells during said reset periods in the remaining subfields without performing said full-surface write discharges, and

executes the erase discharges done separately in said first and second erase discharge periods in the subfields except for said specific subfield.

12. An apparatus according to claim 10, wherein said controller performs the erase discharge for an OFF cell in each said second erase discharge period by applying to a first electrode a first erase pulse whose application voltage continuously changes with time in a positive direction, and applying to a second electrode a second erase pulse whose application voltage continuously changes with time in a negative direction.

13. An apparatus according to claim 12, wherein said controller applies, as said first and second erase pulses, pulse voltages having waveforms whose change rates per unit time of the application voltage change with time.

14. An apparatus according to claim 12, further comprising voltage setting unit for setting the potential difference between the ultimate voltages of said first and second erase pulses to be around the discharge start voltage between said first and second electrodes and to be smaller than said discharge start voltage.

15. An apparatus according to claim 14, wherein said voltage setting unit can change at least one of the ultimate voltages of said first and second erase pulses.

16. An apparatus according to claim 15, wherein said voltage setting unit comprises a first resistor in a pulse generation circuit for generating said first erase pulse and a second resistor in a pulse generation circuit for generating said second erase pulse, and at least one of said first and second resistors is variable.

17. An apparatus according to claim 16, wherein said first and second resistors have different resistance values.

18. An apparatus according to claim 12, wherein said controller synchronizes or delays the rise start timing of said first erase pulse with or from the fall start timing of said second erase pulse.